REMARKS

Claims 2-23 are pending in the above-identified application. Claims 2, 4-5, 7-9, and 11-23 have been amended to delete unnecessary language, to correct dependencies, to make explicit what was inherent, and/or to rephrase the claim language. No new matter has been added.

Claim Objections

Claims 7 and 18 have been objected to as being unclear. The Office action states:

> Pursuant to claims 7 and 18, it is unclear whether the phrase "a derivative circuit design" references the second derivative circuit design or derivative circuit designs within the original circuit design other than the second derivative circuit design.

(March 11, 2003 Office action, pg. 2). Claims 7 and 18 have been amended to make clear that the second derivative circuit design is created by repeating (a) through (e) in claims 2 and 13, respectively, using a derivative circuit design in place of the original circuit design. In other words, the second derivative circuit design is created based upon another derivative circuit design. Applicants respectfully submit that claims 7 and 18, as amended, overcome the objections.

Claim Rejections

Claims 2-23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,175,948 to Miller et al. in view of *ADPCM Codec: From System Level Description to versatile HDL Model* by Herbert Dawid et al.

Claims 2 and 13, as amended, recite "performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprising collecting data on a designer's available experiences and acceptable degree of risk." The Office cites the following passage of Miller as disclosing the claim element:

> The designer creates a functional data flow of the application design 200 from building blocks provided in libraries as referred to in FIG. 1 or creates new ones which can be put into the library. The user designs the application model to meet

> application requirements 220 and constraints 222. Once the models are completed, code can be generated for the equivalent application model and executed on the development platform 210 to verify operation. In the methodology, verification utilities are accommodated such as prints and plots of data resulting from code executing or simulation to assist the designer in determining that the application meets requirements 230 and iterating the process until it does. If the application does not meet requirements, the designer may revise the application model and analyze again.

(Col. 5, l. 58 to col. 6, l. 5).

The cited passage, however, does not disclose or suggest "performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprising collecting data on a designer's available experiences and acceptable degree of risk" as recited in amended claims 2 and 13. Specifically, the cited passage only discloses executing a verification operation after designing the application model. In contrast, front-end acceptance testing is performed on the original circuit design and therefore occurs prior to creating a derivative circuit design. As disclosed in the specification of the above-identified application, front-end acceptance testing may take place even before a designer decides to accept the design project, let alone create a new circuit design. (Para. 0123). Furthermore, Miller does not disclose "collecting data on a designer's available experiences and acceptable degree of risk" during verification.

Dawid describes "how a design flow based on fast system simulation, behavioral synthesis and power analysis is used for the commercial implementation of an ADPCM (Adaptive Differential Pulse Code Modulation) codec module in record time." However, Dawid does not cure the deficiencies of Miller as it also fails to disclose or suggest "performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprising collecting data on a designer's available experiences and acceptable degree of risk" as recited in amended claims 2 and 13. Therefore, even if Miller and Dawid were combined, the combination neither teaches nor suggests "performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprising collecting data on a designer's available experiences and acceptable degree of risk" as recited in amended claims 2 and 13.

Based at least on the above reasons, applicants respectfully submit that claims 2 and 13, as amended, are patentable over Miller in view of Dawid. Given that claims 3-12 and 14-23 depend from claims 2 and 13, respectively, it is respectfully submitted that those claims are patentable over Miller in view of Dawid for at least the same reasons.

CONCLUSION

On the basis of the above remarks, reconsideration and allowance of the claims is believed to be warranted and such action is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

Respectfully submitted,

Bingham McCutchen LLP

Dated: 7-11-03

By: _____
Erin C. Ming
Reg. No. 47,797

Three Embarcadero Center, Suite 1800
San Francisco, CA 94111-4067
Telephone: (650) 849-4904
Telefax: (650) 849-4800